

**ANSHU SINGH**

H. NO. 31 Shastri Puram

Aam wala Tarla Raipur Road

Dehradun, Uttarakhand-248008

Mobile No. 9997802488

Email: anshuaug24@gmail.com

**CAREER OBJECTIVE**

Obtain a teaching career that utilizes my passion for teaching to create a positive experience for the students and coordinating with other teachers to work on interdisciplinary units.

**EDUCATION QUALIFICATIONS**

DEGREE	BOARD/UNIVERSITY	YEAR
PhD.(Organic Electronics)	UTU	Pursuing
M.Tech (VLSI Design)	Faculty of Technology (UTU)	2014-2016
B.Tech (ECE)	GEIT (UTU)	2007-2011
Intermediate	CBSE (D.I.S)	2006
Matriculation	CBSE (K.V.O.F.D)	2004

**SUBJECTS TAUGHT AT U.G LEVEL**

- Microprocessor, Microcontroller and Embedded System
- Digital Electronic and Design Aspects
- Electronic Devices and Circuits, Solid State Devices and Semiconductor Materials
- VLSI Technology, VLSI Circuit Design
- Analog Integrated Circuits and Mobile computing
- Data Communication Networks, Optical Fiber Communication, Digital Communication.

**ACADEMIC EXPERIENCE****Eight Years Academic Experience**

- **Assistant Professor**, Department of Electronics & Communication Engineering, **THDC IHET Sep 2018 to June 2024.**
- **Assistant Professor**, Department of Electronics & Communication Engineering, Doon College of Engineering and Technology (DCET), Saharanpur (U.P), **Jan 2018 to June 2018.**
- **Assistant Professor**, Department of Electronics & Communication Engineering, Indraprastha Institute of Management and Technology (IIMT), Saharanpur (U.P), **Aug 2016 to 30 Dec 2017.**

**TECHNICAL EXPERTISE**

- Organic Electronics, Organic Inverters, Organic Thin Film Transistors, CMOS Design, Semiconductor Device Modeling, Simulation of Electronics Device, Analog & Mixed Signal Circuit Design, Digital Design, Low Power CMOS VLSI Design, Digital electronics, Solid state, Analog electronics, EDC, CAD for VLSI, Analog and Digital Communication.

## **HIGHLIGHTS: QUALIFIED NTA UGC-NET (ELECTRONICS SCIENCE)**

### **CERTIFICATION**

#### **SUMMER TRAINING**

**Project Title** : Image Processing using MATLAB and Thermal Imaging.  
**Organization** : Defence Research and Development Organization, IRDE Dehradun.  
**Period** : 6 Weeks.

### **ACADEMIC PROJECT**

**Ph.D Research Field:** Organic Electronics (Analytical Modeling and Simulation of Electronic Device)

**M.TECH Project Title:** Modeling of Cylindrical OTFT and its Application in Digital Circuits.

**Software of Implementation:** TCAD Silvaco (ATLAS)

**Description:** Cylindrical gate (CG) OTFT has turned out to be promising enough for realizing the circuits that can be amalgamated with textile fabrication line up. These structures are intended for size reduction while simultaneously demonstrating good bending stability, hysteresis free operation and high packing density. Analytical modeling of CG-OTFT is done in different regions. In this research electrical behavior of cylindrical OTFT is examined using 2D Atlas numerical simulators. Moreover this, cylindrical organic thin film transistor are examined. Additionally, we introduce p-type organic inverter-circuits with DLL and ZVLL topology using CG structures.

**B.TECH Project Title:** PIC RF Based Prepaid Energy Meter with Recharge Option.

**Description:** The basic aim of the work to minimize the queue at the electric billing counters and restrict the use of electricity automatically in case bill is not paid. Equipments: 433 MHZ RF transmitter, RF antenna, transformer, LCD, PIC16F877, Relays, integrated circuit.

### **PAPER PRESENTATION**

- Published an International level technical paper on ‘Organic Thin Film Transistor and Organic Inverter based on Cylindrical Gate OTFT’ in International Conference on Emerging Trends in Communication Technologies (ICETCT-2016). In IEEE Xplore digital library.
- Published an International level technical paper on ‘Organic Cylindrical Transistor: Analytical Modeling and Performance Parameters Extraction’ in The ICCCS 2016 International Conference on Communication and Computing Systems Conference.
- Published a International level technical paper on ‘Modeling and Simulation of Cylindrical Gate OTFT and its Application in Digital Circuits’ at IJEDR, 2016 IJEDR Volume 4, Issue 2 ISSN: 2321-9939.

### **PERSONAL DETAILS**

**Name** : Anshu Singh  
**Father's Name** : Mr. Desh Raj  
**Date of Birth** : 24<sup>th</sup> August, 1988  
**PAN NO.** : CIIPS8731A  
**Nationality** : Indian  
**Sex** : Male  
**Marital Status** : Married  
**Hobbies** : Bicycle riding, Design of basic electronic circuits, Playing Cricket.

I hereby declare that above information given by me is true to best of my knowledge.

**Place:** Dehradun

**Date:** 08/08/2024

**(ANSHU SINGH)**